REMARKS

The Examiner is thanked for the performance of a thorough search.

In this reply, Claims 1, 36, and 45 have been amended. Claims 5, 6, 8, 9, and 14-35 were previously canceled. Claims 1-4, 7, 10-13, and 36-45 are pending in the application.

CLAIM REJECTIONS – 35 U.S.C. § 101

The Office Action rejected Claims 36-44 under 35 U.S.C. §101. Claim 36 has been amended to recite a "tangible" computer-readable medium. Claims 37-66 inherit this tangibility from Claim 36 due to their dependence from Claim 36. Withdrawal of the rejection of Claims 36-44 under 35 U.S.C. §101 is respectfully requested.

CLAIM REJECTIONS – 35 U.S.C. § 102

The Office Action rejected Claims 1, 2, 36, 37, and 45 under 35 U.S.C. § 102(e) as being anticipated, allegedly, by U.S. Patent No. 6,862,635 to Alverson, et al. ("Alverson"). Claims 1, 36, and 45 have been amended.

Claim 1 requires determining, at a particular time, whether a buffer array entry indicates a particular value. The Office Action appears to analogize the "particular value" to Alverson's "full/empty bit," or, alternatively, to Alverson's "pointer to an item removed from the parallel list" (referred to simply as "the pointer" below).

Claim 1 further requires performing alternative steps based on whether the buffer array entry indicates the particular value at the particular time. If the entry indicates the particular value at the particular time, then an attempt is made to obtain a lock on a particular data buffer that is associated with the buffer array entry. Alternatively, if the

entry does not indicate the particular value at the particular time, then no such attempt is made, and a buffer index value is incremented.

Although it is not expressly stated in Claim 1, the avoidance of attempting to obtain a lock on a particular data buffer (in the case that the buffer array entry for that buffer indicates the particular value) advantageously eliminates overhead problems from which Alverson's disclosed technique suffers; instead of attempting to obtain a lock on a data buffer that is likely to be "in use," or "blocking" until the data buffer is no longer "in use," a different data buffer corresponding to a subsequent buffer index value can be tried. In stating this advantage of the method of Claim 1, the Applicants are not trying to argue that Claim 1 should be interpreted based on text that is not expressly recited in Claim 1; the Applicants merely wish to express the significance of the difference between the method of Claim 1 and Alverson's disclosed technique. The difference is explained below.

In Claim 1, alternative steps are performed depending on the outcome of the recited determination—depending on whether the buffer array entry indicates the particular value at the particular time. **Either** an attempt to obtain a lock is made **or** a buffer index value is incremented. However, in Alverson, **neither** of the actions alleged to be analogous to attempting to obtain a lock and incrementing the buffer index value has anything to do with whether the "full/empty bit" is set. Additionally, in Alverson, **neither** of the actions alleged to be analogous to attempting to obtain a lock and incrementing the buffer index value has anything to do with the value of the pointer.

The last limitation of Claim 1 will be used as a more specific example to explain the difference between Claim 1 and Alverson. This limitation says, "if the buffer array entry indicates the particular value at the particular time, then, in response to a determination **at the particular time** that the buffer array entry indicates the particular

value, **incrementing the buffer index value without attempting to obtain a lock on the particular data buffer**."

Suppose momentarily that Alverson's "full/empty bit" is analogous to the "particular value." Suppose, initially, that the bit's value is "**empty**" at the particular time that the determination of the bit's value is made. In this case, in step 1401, the write counter is incremented; the Office Action analogizes this to "incrementing the buffer index value." Then, in step 1403, the "read" blocks. According to Alverson, step 1403 "effects locking" of the bucket, and the Office Action analogizes this to "attempting to obtain a lock." Therefore, in the case that the bit's value is "empty" at the particular time, **both** the actions (the actions that the Office Action analogizes to incrementing the buffer index value and attempting to obtain the lock) are performed.

Continue supposing that Alverson's "full/empty bit" is analogous to the particular value. This time, though, suppose that the bit's value is "**full**" at the particular time that the determination of the bit's value is made. In this case, in step 1401, the write counter is still incremented. Therefore, whether or not the write counter is incremented has nothing to do with the bit's value. Then, in step 1403, the "read" succeeds. Even so, according to Alverson, step 1403 "effects locking" of the bucket, which the Office Action analogizes to "attempting to obtain a lock." Therefore, whether or not "locking" of the bucket is "effected" has nothing to do with the bit's value; regardless of whether the bit is "empty" or "full" at the particular time that the bit's value is determined, the action that the Office Action analogizes to "attempting to obtain a lock" will still be performed. Therefore, in the case that the bit's value is "full" at the particular time, **both** the actions (the actions that the Office Action analogizes to incrementing the buffer index value and attempting to obtain the lock) are performed.

Therefore, it is clear that regardless of whether the "full/empty bit" is "empty" or "full" at the time that the bit's value is determined, **both** the actions will be performed. In contrast, Claim 1 recites that if "if the buffer array entry **indicates the particular value at the particular time**, then, in response to a determination at the particular time that the buffer array entry indicates the particular value, **incrementing the buffer index value without attempting to obtain a lock on the particular data buffer**." There is no value of the "full/empty bit" that will cause the technique disclosed in Alverson to perform step 1401 (allegedly analogous to "incrementing the buffer index value") without performing step 1403 (allegedly analogous to "attempting to obtain a lock on the particular data buffer").

As discussed above, the Office Action also appears to analogize the "buffer index value" of Claim 1 to the pointer of Alverson. According to Alverson, the pointer is either NULL or it points to an item removed from the parallel list. In either case, though, the "read counter" is incremented in block 1503, and the "locking" of the bucket is "effected" in block 1507. There is no value of the pointer that will cause the technique disclosed in Alverson to perform step 1503 (allegedly analogous to "incrementing the buffer index value") without performing step 1507 (allegedly analogous to "attempting to obtain a lock on the particular data buffer").

Therefore, Alverson fails to disclose "if the buffer array entry indicates the particular value at the particular time, then, in response to a determination **at the particular time** that the buffer array entry indicates the particular value, **incrementing the buffer index value without attempting to obtain a lock on the particular data buffer**" as recited in Claim 1. For at least this reason, Claim 1 is patentable over Alverson under 35 U.S.C. § 102(e).

By virtue of its dependence from Claim 1, Claim 2 comprises the limitations of Claim 1 that are distinguished from Alverson above. Therefore, Claim 2 is also patentable over Alverson under 35 U.S.C. § 102(e).

As noted in the Office Action, Claims 36, 37, and 45 correspond to one or the other of Claims 1 and 2. Therefore, Claims 36, 37, and 45 are also patentable over Alverson under 35 U.S.C. § 102(e).

If a future Office Action maintains the rejections of these claims under similar grounds, it is respectfully requested that the Office Action expressly state which specific elements disclosed in Alverson are alleged to correspond to the "buffer index value" and "the particular value" of Claim 1.

CLAIM REJECTIONS – 35 U.S.C. § 103

The Office Action rejected Claims 3, 4, 7, 10-13, and 38-44 under 35 U.S.C. § 103(a) as being unpatentable, allegedly, over Alverson in view of U.S. Patent No. 6,182,086 to Lomet, et al. ("Lomet").

Claims 3, 4, 7, 10-13, and 38-44 each depend from various ones of the independent claims discussed above. By virtue of their dependence from these independent claims, Claims 3, 4, 7, 10-13, and 38-44 comprise the limitations of the independent claims that are distinguished from Alverson above.

The Office Action does not rely on Lomet to disclose the limitations distinguished from Alverson above. The Office Action relies on Lomet only to disclose, allegedly, other limitations. Since neither Lomet nor Alverson discloses, teaches, or suggests the distinguished limitations, even the combination of Lomet and Alverson does not disclose, teach, or suggest the distinguished limitations.

Therefore, Claims 3, 4, 7, 10-13, and 38-44 are patentable over Alverson and Lomet under 35 U.S.C. § 103(a).

CONCLUSION

Applicant believes that all issues raised in the Office Action have been addressed and that allowance of the pending claims is appropriate. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

The Examiner is invited to telephone the undersigned at (408) 414-1080 to discuss any issue that may advance prosecution. To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. § 1.136. The Commissioner is authorized to charge any fee that may be due in connection with this Reply to our Deposit Account No. 50-1302.

Respectfully submitted,

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